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(PTO ASSISTANCE)

Application : 09/993778 Examiner : Rodriguez GAU : 2851

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<input checked="" type="checkbox"/> SPEC	<u>11-5-2001</u>	

[RUSH] MESSAGE:

Page 18, line 16 of the specification is missing data

Thank you

[XRUSH] RESPONSE:

See misc comm

Done

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NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

RICHARD O. GRAY, JR.
JEFFREY T. HALEY
STEPHEN M. EVANS
JOSHUA KING
BRYAN A. SANTARELLI
PAUL F. RUSYN
JOHN M. JANEWAY
PAUL G. LUNN
J. MARK HAN*
NOT LICENSED IN WASHINGTON

LAW OFFICES OF

GRAYBEAL JACKSON HALEY LLP
Attorneys at Law

155 - 108TH AVENUE N.E., SUITE 350
BELLEVUE, WASHINGTON 98004-5973
TELEPHONE: (425) 455-5575
FACSIMILE: (425) 455-1046
WWW.GRAYBEAL.COM

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February 6, 2006

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From: Bryan A. Santarelli

Our Ref: 01-S-054 (1678-49)

Regarding: Response to Notice to File Corrected Application Papers

Message: Please see attached.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Fereidoon Heydari, Hakan Ozdemir, and Sadik O. Arf

Title: SERVO CIRCUIT HAVING A SYNCHRONOUS SERVO CHANNEL
AND METHOD FOR SYNCHRONOUSLY RECOVERING SERVO
DATA

Serial Number: 09/993,778

Filing Date: November 5, 2001

Examiner/Unit: Glenda P. Rodriguez / 2837

Attorney Docket No.: 01-S-054 (1678-49)

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RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

February 3, 2006

TO THE COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Notice to File Corrected Application Papers mailed January 9,
2006, the Applicants' attorney requests amendment of the above-referenced application as
follows.

I. AMENDMENT

In the Specification:

[62] Referring to **FIGS. 4 – 7** and **9**, during normal operation the disk-drive controller (**FIG. 20**), transitions SG to an active level at time T_{12} , which is when the controller determines that the read-write head (**FIG. 5**) is at the beginning of a servo wedge **22**. In response to SG having an active level, the processor **40** causes the circuits **36** and **58** to calculate initial phase and gain values for α_1 and Y as described above. After a first predetermined delay, which is 16 samples in one embodiment, the processor **40** causes the sample-interpolator loop **54** and gain circuit **38** to enter the acquisition mode as described above. Then, after a second predetermined delay that in one embodiment equals the latency of the loop **54**, the processor **40** transitions ACQ_TRK to an active level at time t_{13} and causes the loop **54** and circuit **38** to enter the tracking mode as described above. The processor **40** recovers the SSM **76** at time t_{14} , and in response transitions SRV_SMD to an active level SG and ACQ_TRK remain active from time t_4 until time t_5 , which is long enough for the servo channel **34** to read the servo data in the servo wedge **22**.

II. REMARKS

Claims 1-23 are pending and allowed, and the Issue Fee was paid on December 12, 2005. As required by the Notice to File Corrected Application Papers, Applicants have amended paragraph 62 to fill in the missing data.

Conclusion

In light of the foregoing, and in addition to the allowed claims 1-23, please pass this application along for issuance.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 3rd day of February, 2006.

Respectfully Submitted,

GRAYBEAL JACKSON HALEY LLP



Bryan A. Santarelli
Attorney for Applicant
Registration No. 37,560
155 - 108th Ave. NE, Suite 350
Bellevue, WA 98004-5973
(425) 455-5575



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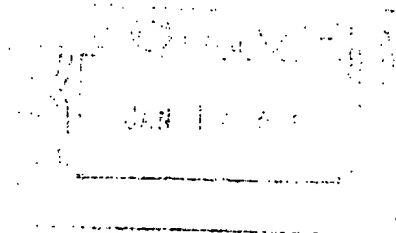
APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,778	11/05/2001	Fereidoon Heydari	01-S-054 (1678-49)	7609
30431	7590	01/09/2006	EXAMINER	
STMICROELECTRONICS, INC. MAIL STATION 2346 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006			RODRIGUEZ, GLENDA P	
			ART UNIT	PAPER NUMBER
			2651	

DATE MAILED: 01/09/2006

due 2/9/06

Please find below and/or attached an Office communication concerning this application or proceeding.

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Serial Number
09993778

Date Mailed
1/09/06

NOTICE TO FILE CORRECTED APPLICATION PAPERS***Notice of Allowance Mailed***

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given 30 days from the mail date of this Notice within which to correct the informalities indicated below. A failure to reply will result in the application being ABANDONED. This period for reply is NOT extendable under 37 CFR 1.136 (a) or (b).

- ♦ Specification page 18, line 16 has missing data. Fax missing information to number below or e-mail.
 - For status updates visit <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR System, contact the Electronic Business Center (EBC) toll free at 866-217-9197.

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A handwritten signature in black ink, appearing to read "Rori Burch", written over a horizontal line.

Rori Burch
USPTO
Publishing Division
Rori.burch@uspto.gov
Fax (571) 273-9009
Fax (703) 308-6642
703-305-0333 ext.135 (V)

Docket 01-S-054 (1678-49)

then SEARCH remains at an active level, and the processor 40 resets SMD_CNT and re-executes the spin-up detection procedure from the beginning until it recovers the desired number of consecutive SSMs 76. Furthermore, although the recovered consecutive SSMs 76 are typically within the same track 14, this is not required.

5 [61] FIG. 9 is a timing diagram of the signals of FIG. 8 during post-spin-up, i.e., normal, operation of the servo circuit 30 of FIG. 5 according to an embodiment of the invention. SEARCH, PDETECT, and SMD_CNT are inactive during normal operation. A major difference between spin-up and normal operation is that the preamble detection algorithm is not used during normal operation because the disk-drive controller (FIG. 10 "knows" the position of the read-write head (FIG. 5).

03 [62] Referring to FIGS. 4 – 7 and 9, during normal operation the disk-drive
04 controller (FIG. 20), transitions SG to an active level at time T_{12} , which is when the
05 controller determines that the read-write head (FIG. 5) is at the beginning of a servo
06 wedge 22. In response to SG having an active level, the processor 40 causes the
15 circuits 36 and 58 to calculate initial phase and gain values for α_1 and Y as described
07 above. After a first predetermined delay, which is ____ in one embodiment, the
08 processor 40 causes the sample-interpolator loop 54 and gain circuit 38 to enter the
09 acquisition mode as described above. Then, after a second predetermined delay that in
10 one embodiment equals the latency of the loop 54, the processor 40 transitions
20 ACQ_TRK to an active level at time t_{13} and causes the loop 54 and circuit 38 to enter
the tracking mode as described above. The processor 40 recovers the SSM 76 at time
 t_{14} , and in response transitions SRV_SMD to an active level SG and ACQ_TRK remain
active from time t_4 until time t_6 , which is long enough for the servo channel 34 to read
the servo data in the servo wedge 22.

25 [63] FIG. 10 is a block diagram of the sample-interpolator loop 54 — which is sometimes called a digital-baud-rate-timing-recovery circuit — of FIG. 5 according to an embodiment of the invention. Although details of the circuit 54 are discussed below, further details are disclosed in commonly owned U.S. Patent App. Ser. No. 09/387,146.